DISPLAY CORPORATION

SPECIFICATION

Customer:

Model Name: FB101EHV401-A

Date: 2019/03/14

Version: 0.2

☐ Preliminary Specification

■ Final Specification

Remark
10.1D LCM (LVDS)

For Customer's Acceptance

Approved by	Comment

Approved by	Reviewed by	Prepared by
JAMES LI 2019/03/14		XL HAN 2019/03/14

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RECORD OF REVISION

Version	Revise Date	Page	**Description**
0.1	2018/09/07	All	New

1. FEATURES

FB101EHV401-A is a transmissive type color active matrix liquid crystal display (LCD),which uses amorphous thin film transistor (TFT) as switching devices. This panel has a 10.1 inches diagonally measured active display area with 1024 x 600 resolution. This product is composed of a TFT LCD panel, Polarizers, driver ICs and FPC.

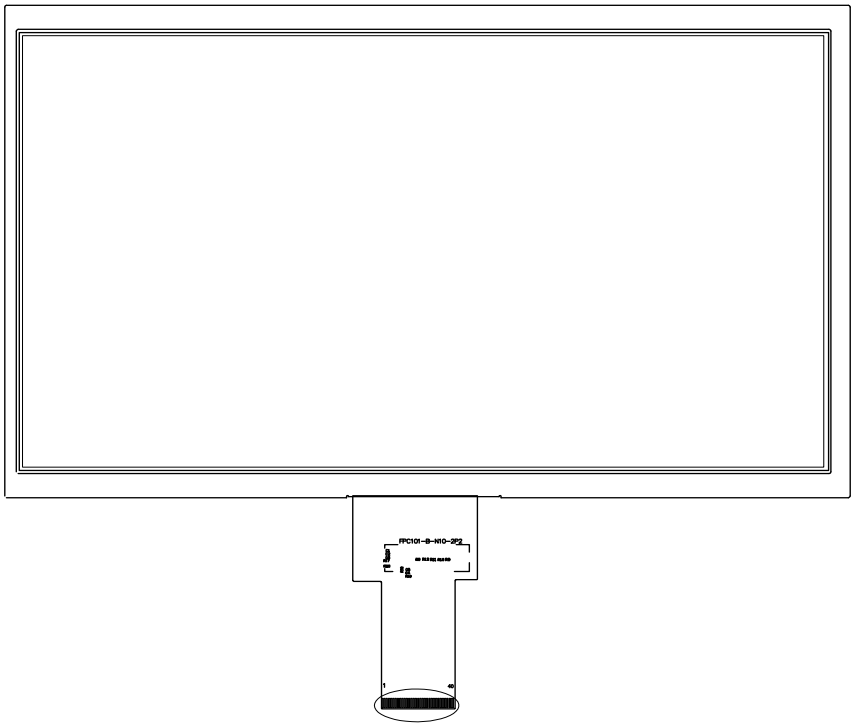
2. GENERAL SPECIFICATIONS

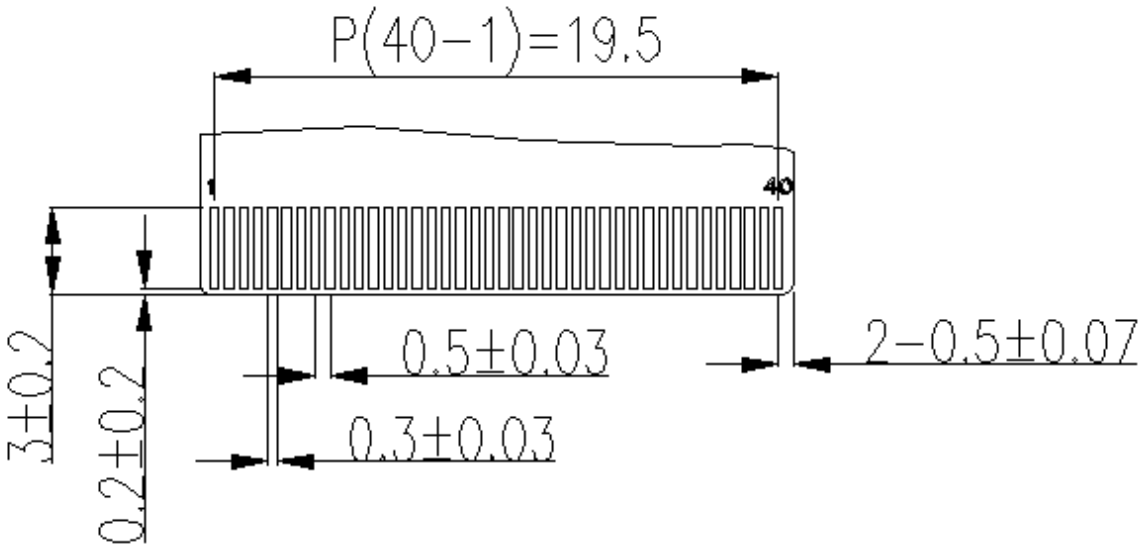
Item	Description	Unit
Display Size	10.1	inch
Display Type	Transmissive, a-Si	-
Active Area (HxV)	222.72 (H) x 125.28 (V)	mm
Number of Dots (HxV)	1024 x RGB x 600	dot
Pixel Pitch(HxV)	0.2175 x 0.2088	mm
Color Arrangement	RGB Stripe	-
Color Numbers	16.7 M	-
Transmissive Mode	Normally black	-
Outline Dimension (HxVxT)	235 (H) x 143 (V) x 5.0 (D)	mm
NTSC (CIE1931) (Under C light)	53(Typ.)	%
Response Time	≤35	ms
Viewing Angle (Light On) (R/U/L/D)	CR≧10 @ R/L/U/D(80°/80°/80°/80°) (Typ.)	
Surface Treatment	HC	
Contrast Ratio (Light On)	800:1 (Typ)	
Operation Temperature	-20~70	℃
Storage Temperature	-30~70	℃
Interface	LVDS	
Luminance	450	cd/m^2

3. Pin Description

3.1 Golden finger

PIN pitch = 0.5mm





3.2 PIN Assignment

No	Symbol	I/O	Function	Remark
1	VCOM	P	Common Voltage	
2	VDD	P	Power Voltage for digital circuit	
3	VDD	P	Power Voltage for digital circuit	
4	NC	-	No connection	
5	RESET	I	Global reset pin	
6	STBYB	I	Standby mode, Normally pulled high STBYB = “1”, normal operation STBYB = “0”, timing controller, source driver will turn off, all output are High-Z	
7	GND	P	Ground	
8	RXIN0-	I	LVDS differential data input 0-	
9	RXIN0+	I	LVDS differential data input 0+	
10	GND	P	Ground	
11	RXIN1-	I	LVDS differential data input 1-	
12	RXIN1+	I	LVDS differential data input 1+	
13	GND	P	Ground	
14	RXIN2-	I	LVDS differential data input 2-	
15	RXIN2+	I	LVDS differential data input 2+	
16	GND	P	Ground	
17	RXCLKIN-	I	LVDS differential clock input -	
18	RXCLKIN+	I	LVDS differential clock input +	
19	GND	P	Ground	
20	RXIN3-	I	LVDS differential data input 3-	
21	RXIN3+	I	LVDS differential data input 3+	
22	GND	P	Ground	
23	NC	-	No connection	
24	NC	-	No connection	
25	GND	P	Ground	
26	NC	-	No connection	

27	PWMO	O	Backlight CABC controller signal output	
28	SELB	I	6bit/8bit mode select	Note 1
29	AVDD	P	Power for Analog Circuit	
30	GND	P	Ground	
31	NC	-	No connection	
32	NC	-	No connection	
33	L/R	I	Horizontal inversion	Note 3
34	U/D	I	Vertical inversion	Note 3
35	VGL	P	Gate OFF Voltage	
36	CABCEN1	I	CABC H/W enable	Note 2
37	CABCEN0	I	CABC H/W enable	Note 2
38	VGH	P	Gate ON Voltage	
39	NC	-	No connection	
40	NC	-	No connection	

I: input, O: output, P: power

Note1: If LVDS input data is 6 bits, SELB must be set to High;

If LVDS input data is 8 bits, SELB must be set to Low.

Note2: When CABC_EN=”00”, CABC OFF.

When CABC_EN=”01”, user interface image.

When CABC_EN=”10”, still picture.

When CABC_EN=”11”, moving image.

When CABC off, don’t connect DIMO, else connect it to backlight.

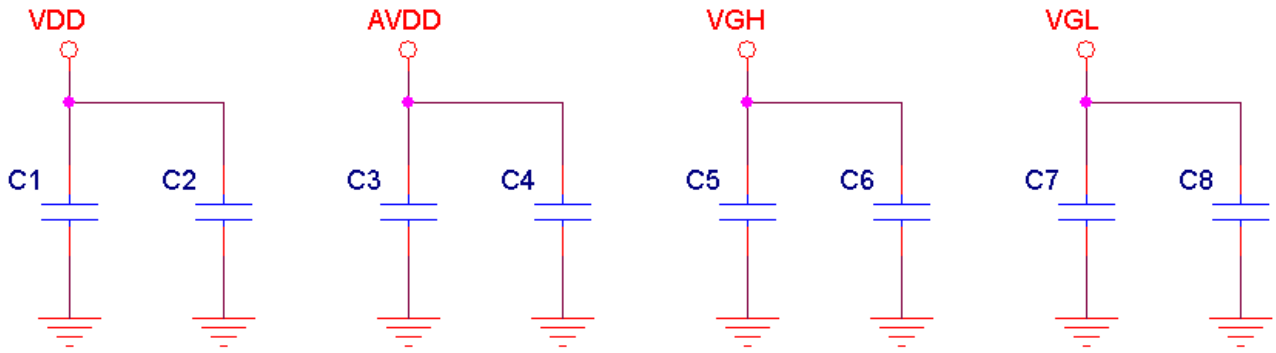
Note 3: Selection of scanning mode

Setting of scan control input		Scanning direction
U/D	L/R	
GND	VDD	Up to down, left to right
VDD	GND	Down to up, right to left
GND	GND	Up to down, right to left
VDD	VDD	Down to up, left to right

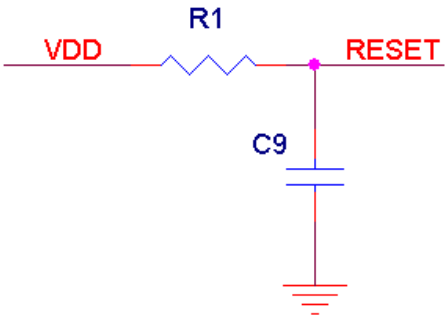
Definition of scanning direction .Refer to the figure as below

3.3 Advice circuit for customer system

3.3.1 Power PIN: AVDD/VDD/VGH/VGL

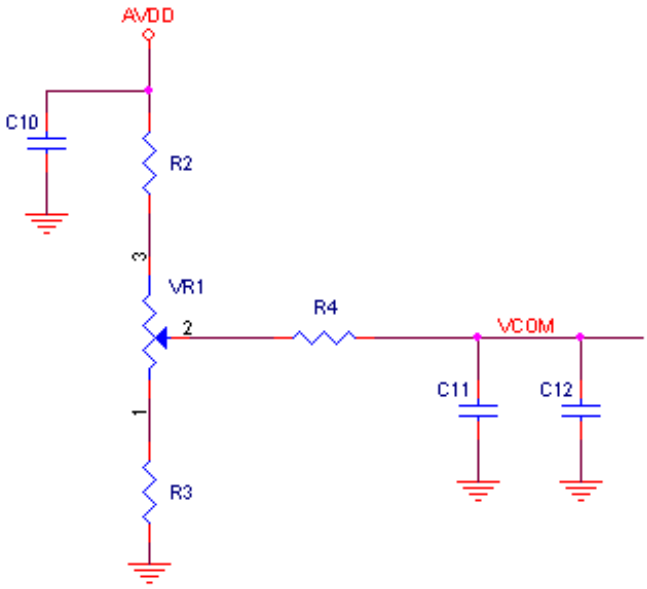


3.3.2 Control PIN: RESET



3.3.3 VCOM

Typical VCOM is only a reference value, it must be optimized according to each LCM. Be sure to use VR;



3.3.4 Suggestion BOM

Location	Description
C1,C11	10uF,X5R,10V
C2,C12	100nF,X5R,10V
C3,C7	10uF,X5R,25V
C4,C8	100nF,X5R,25V
C5	10uF,X5R,50V
C6	100nF,X5R,50V
C9	1uF,X5R,10V
C10	1uF,X5R,25V
R1	10Kohm,1%
R2	12Kohm,1%
R3	10Kohm,1%
R4	0ohm,1%
VR1	10Kohm,1%

4. ABSOLUTE MAXIMUM RATING

Item	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	VDD	-0.3	3.6	V	
	AVDD	-0.3	15	V	
	VGH	-0.3	30	V	
	VGL	-15	0.3	V	
Storage temperature	Tstg	-30	+70	℃	
Operating Temperature	Topr	-20	+70	℃	

Note:

(1) All of the voltages listed above are with respective to GND= 0V

(2) Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

5. DC CHARACTERISTICS

5.1 Parameter

Item	Symbol	Value			Units	Remark
		Min	Typ	Max		
Power supply voltage	VDD	3.0	3.3	3.6	V	
	AVDD	9.2	9.6	10	V	
	VGH	17	18	19	V	
	VGL	-5.5	-6	-6.5	V	
Input signal voltage	VCOM	4	4.1	4.4	V	
Ripple Voltage	VRP	-	50	100	mV	Note 1
Logic high level input voltage	VIH	0.7xVDD	-	VDD	V	Note 2
Logic low level input voltage	VIL	VSS	-	0.3xVDD	V	

(Ta = 25 ± 2℃)

Note 1: Including signal: VDD、AVDD、VGH、VGL、VCOM.

Note 2: Including signal: U/D、L/R、RESET、STBYB、SELB、CABCEN0、CABCEN1.

5.2 Current Consumption

Item	Symbol	Value			Units	Remark
		Min	Typ	Max		
Current for Driver	IVDD	4	15	20	mA	Note 1
	IAVDD	8	45	65	mA	Note 1
	IVGH	0.1	0.6	2	mA	Note 1
	IVGL	0.1	0.6	2	mA	Note 1

Note 1：The specified power supply current is under the conditions at VDD=3.3V，AVDD=12.2V，VGH=22V，VGL=-10V, Ta = 25 ± 2 ºC, DC Current and fv = 60 Hz, whereas a power dissipation check white pattern.

5.2.1. Backlight Driving Conditions

ITEM	SYMBOL	VALUES			UNIT	REMARK
		MIN.	TYP.	MAX.		
Voltage for LED backlight	V_L	15.0	15.5	16.5	V	Note 1
Current for LED backlight	I_L	-	140	150	mA	-
LED life time	-	30,000	-	-	Hr	Note 2

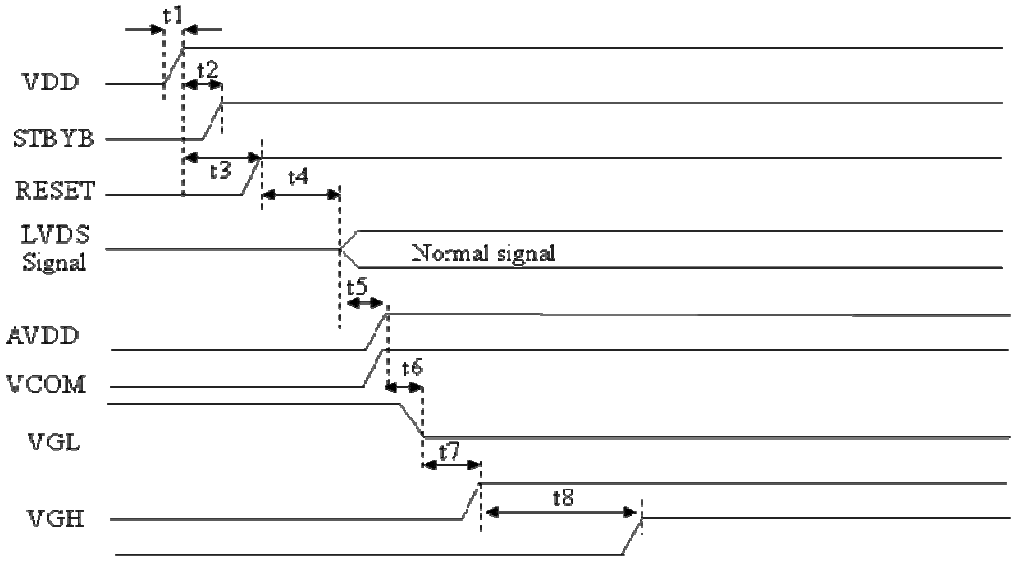
Note 1: The LED Supply Voltage is defined by the number of LED at Ta=25℃ and I_L = 140mA.

Note 2: The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and I_L = 140mA.

The LED lifetime could be decreased if operating I_L is lager than 140mA.

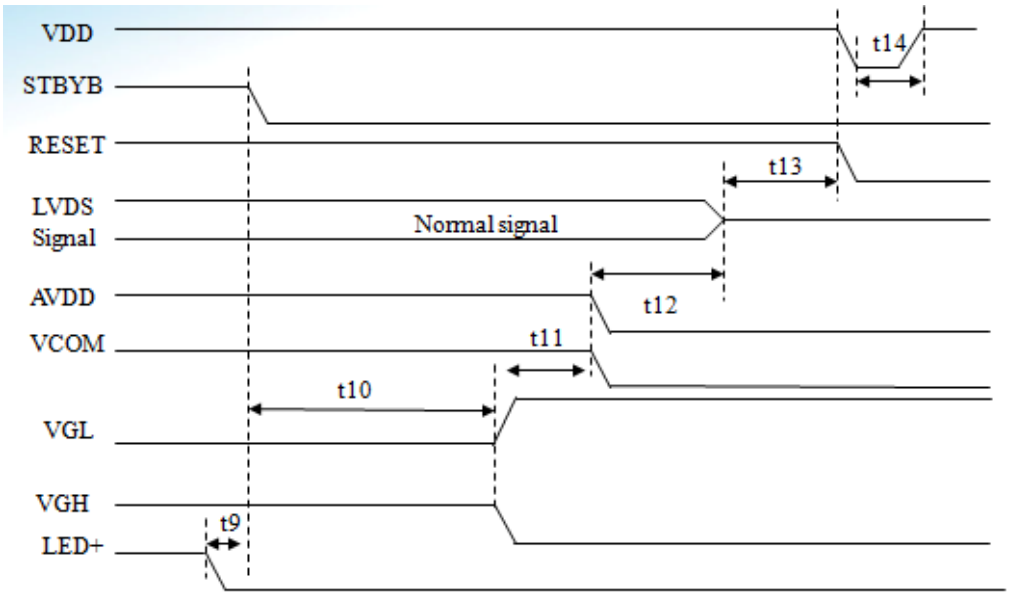
5.3 Power Sequence

Power on



Symbol	SPEC			Unit
	Min.	Typ.	Max.	
t1	1	10	20	ms
t2	20	35	50	us
t3	1	10(RC Delay)	12	ms
t4	30	50	100	ms
t5	0.1	5	20	ms
t6	20	70	120	ms
t7	40	90	140	ms
t8	150	170	200	ms

Power off



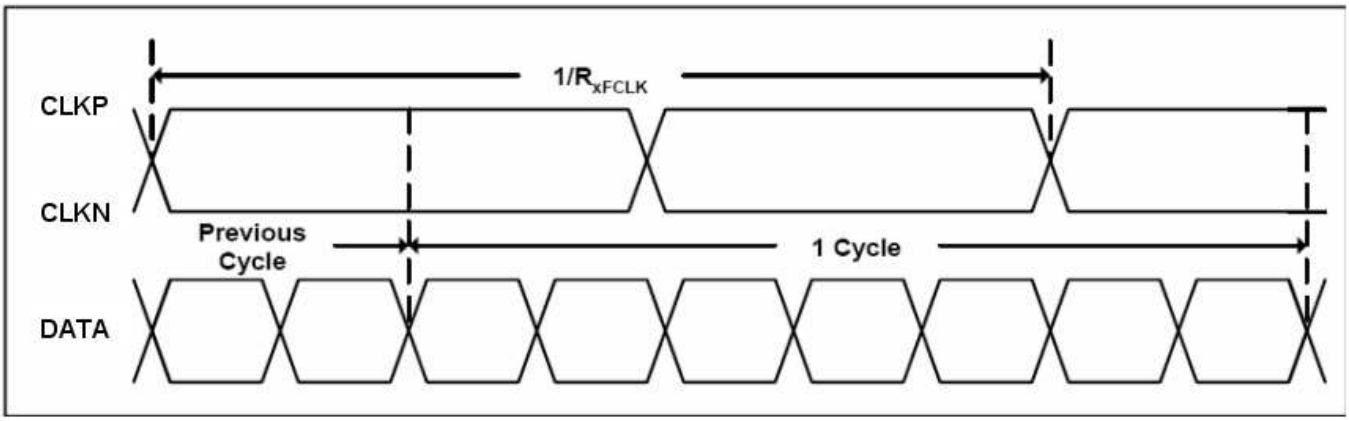
Symbol	SPEC			Unit
	Min.	Typ.	Max.	
t9	0.1	1	10	ms
t10	120	150	200	ms
t11	50	100	200	ms
t12	1	10	20	ms
t13	0.1	10	100	ms
t14	500	-	-	ms

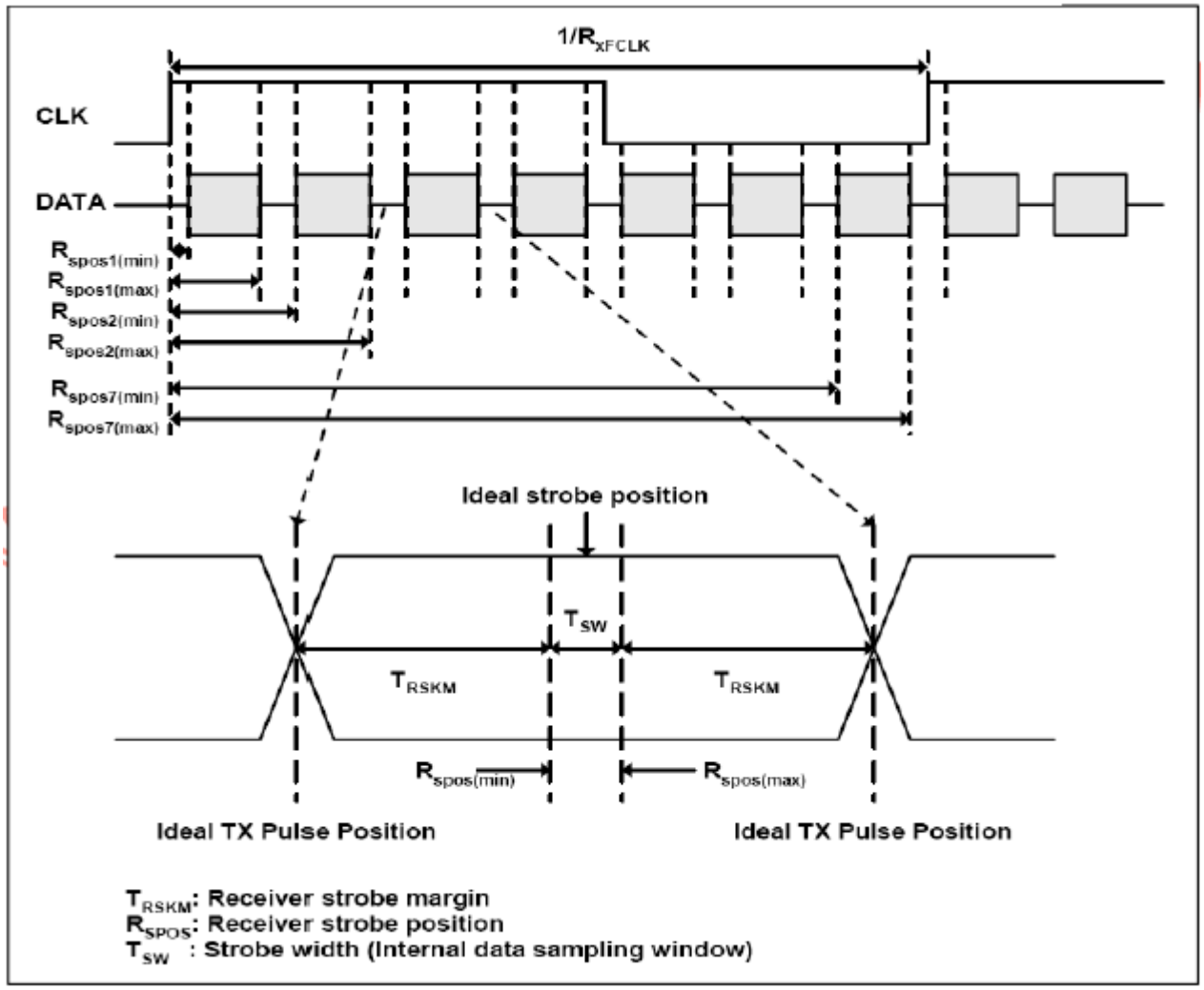
6. Timing Characteristics

6.1 AC Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Clock frequency	RxFCLK	26.2	51.2	71	MHz	
Input data skew margin	TRSKM	500	500	1/(2*RxFCLK)	ps	Typical value for 1024*600 resolution
Clock high time	TLVCH	4/(7xRxFCLK)			ns	|VID|=400mv RxVCM=1.2V RxFCLK=71MHz VDD_LVDS=3.3V
Clock low time	TLVCL	3/(7xRxFCLK)			ns	
VSD setup time	TenPLL	0<TenPLL<150			us	

6.2 Input Clock and Data Timing Diagram

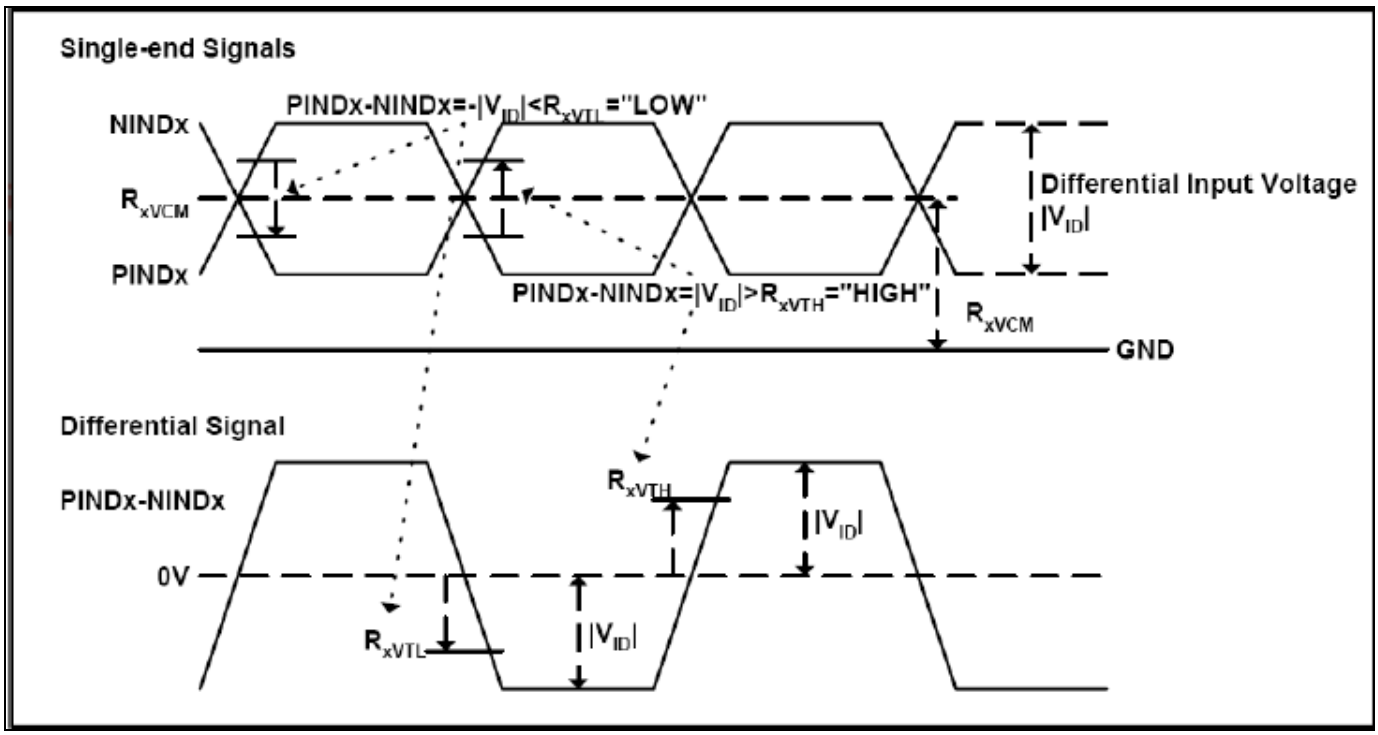




6.3 Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Differential input high threshold voltage	RxVTH	0.1	0.2	|VID|	V	RxVCM=1.2V
Differential input low threshold voltage	RxVTL	-|VID|	-0.2	-0.1	V	
Input voltage range (singled-end)	RxVIN	0	1.2±0.4	2.4	V	
Differential input common mode voltage	RxVCM	|VID|/2	1.2	2.1-|VID|/2	V	
Differential input voltage	|VID|	0.2	0.4	0.6	V	
Differential input leakage current	RVxIiz	-10	0	+10	uA	

LVDS Digital Operating Current	Iddlvds	8	22	30	mA	Fclk=65MHz,VDD=3.3V
LVDS Digital Standby Current	Istlvds	0	200	300	uA	Clock & all Functions are stopped
LVDS Differential impendence	Zdiff	90	100	110	ohm	RXINx+/-, RXINCLK+/-

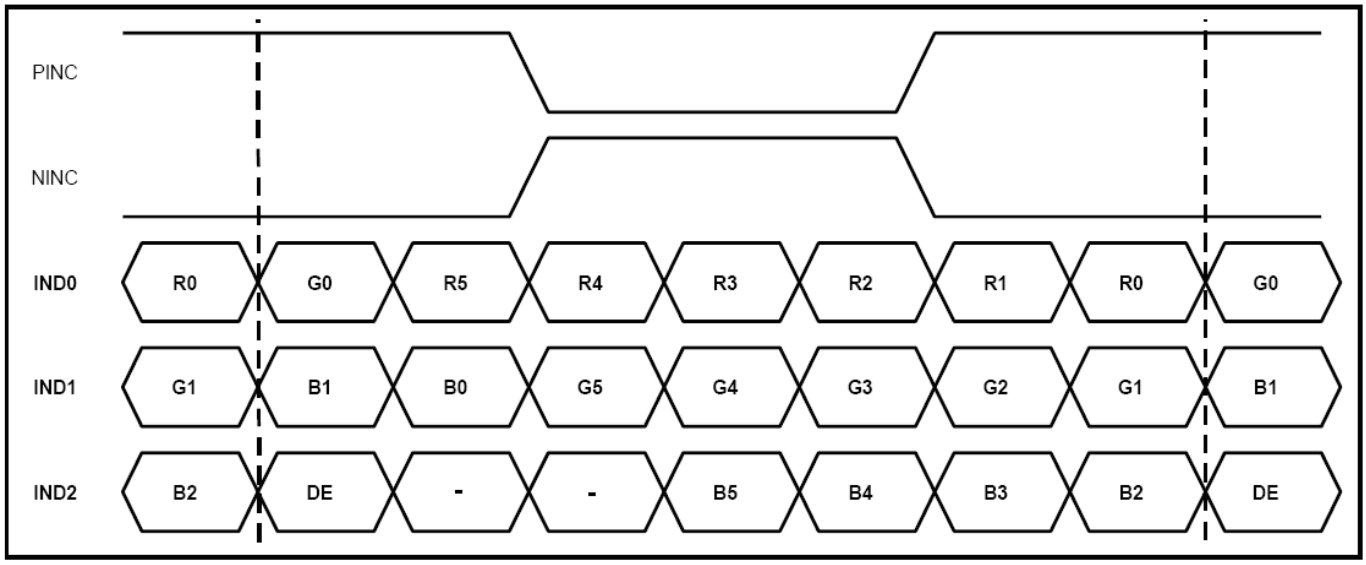


6.4 Timing

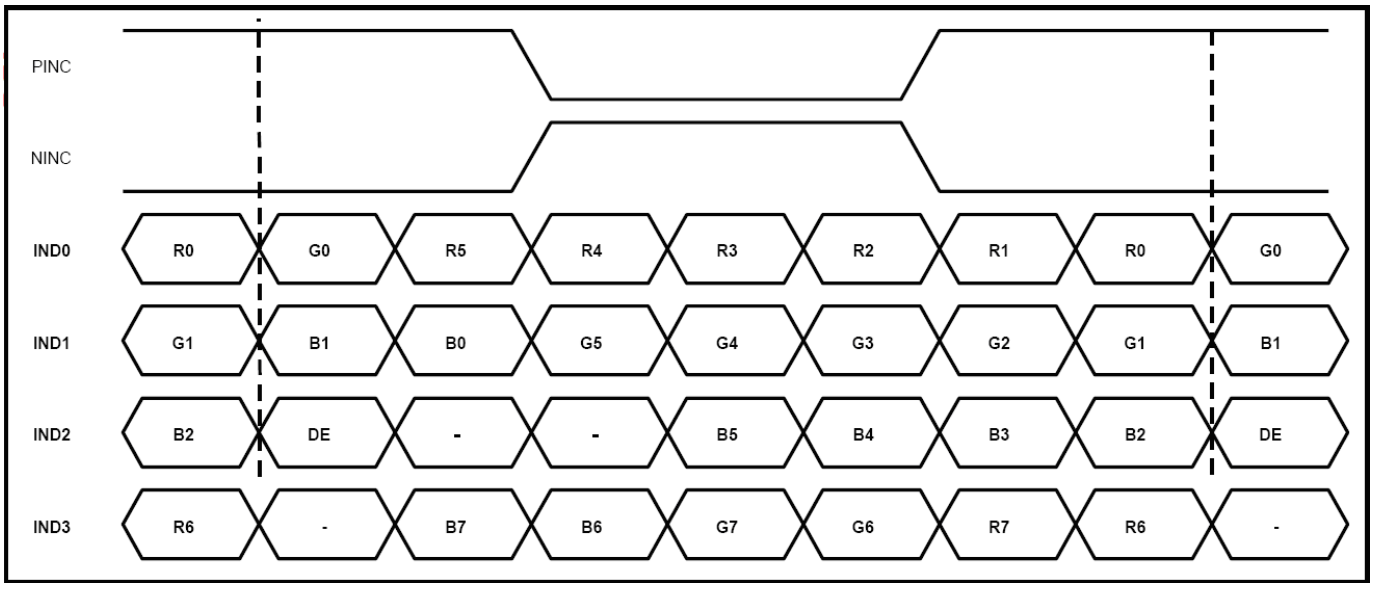
Parallel	Symbol	Vaule			Unit
		Min	Typ	Max	
DCLK Freqency Frame rate=60Hz	fclk	42.5	51.2	67.2	MHz
Horizontal display area	thd		1024		DCLK
HSYNC period time	thpw	1164	1344	1400	DCLK
HSYNC blanking	thb+thfp	140	320	376	DCLK
Vertical display area	tvd		600		H
VSYNC period time	tvpw	610	635	800	H
VSYNC blanking	tvb+tvfp	10	35	200	H

6.5 Data Input Format

6bit LVDS input



8bit LVDS input



7. OPTICAL CHARACTERISTICS

7.1 Optical Specification

Ta=25℃

Item	Symbol		Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles	Θ11(R)		CR ≥ 10	75	80	-	Degree	Note 7-1
	Θ12(L)			75	80	-		
	Θ21(U)			75	80	-		
	Θ22(D)			75	80	-		
Response Time	Tr+Tf		Θ=0°	-	25	35	ms	Note 7-2
Transmittance	T			4.97	5.54	-	%	Note 7-3
Contrast Ratio	CR			600	800	-	-	Note 7-4
Chromaticity	White	x		0.303	0.333	0.363	-	*C Light Source* Note 7-5
		y		0.332	0.362	0.392		
	Red	x		0.597	0.627	0.657		
		y		0.318	0.348	0.378		
	Green	x		0.275	0.305	0.335		
		y		0.511	0.541	0.571		
	Blue	x		0.106	0.136	0.166		
		y		0.087	0.117	0.147		
NTSC	-			48	53	-	%	

7.2 Basic measure condition

(1) Driving voltage

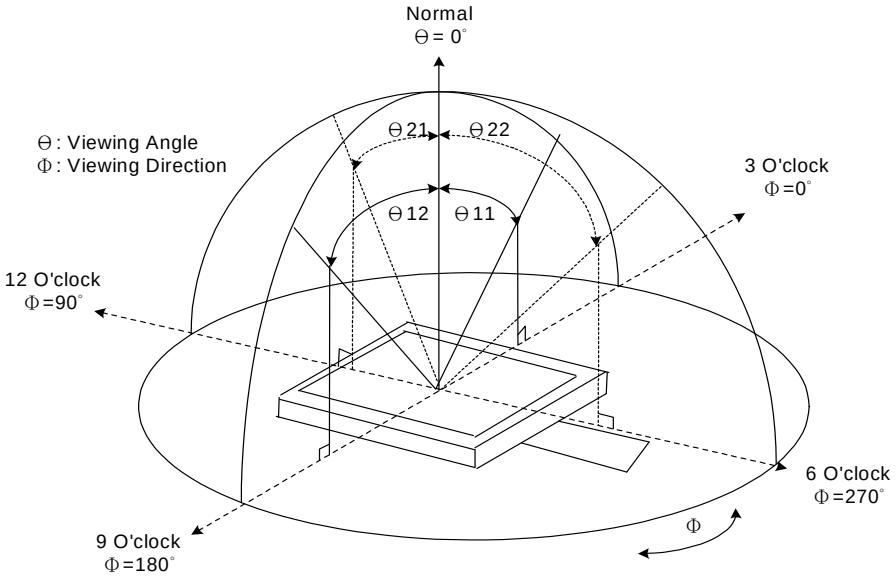
Based on item 5. DC CHARCTERISTICS and 6. AC CHARCTERISTICS

(2) Ambient temperature: Ta=25℃

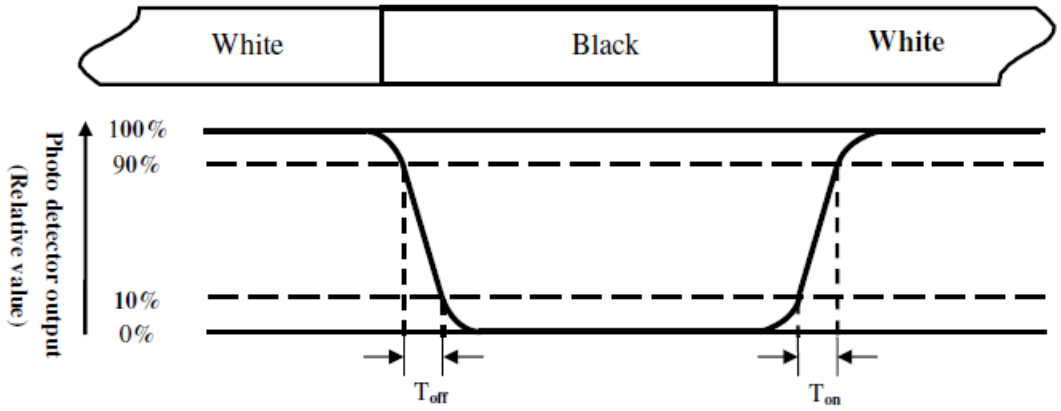
(3) Testing point: measure in the display center point and the test angle Θ=0°

(4) Testing Facility: Environmental illumination: ≤ 1 Lux

Note 7-1: Viewing angle diagrams



Note 7-2: Response time



Note 7-3: Transmittance

The transmittance is measured on INX stabilized backlight.

Note 7-4: Contrast ratio

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = White / Black

Note 7-5 Chromaticity

The chromaticity is measured in CIE 1931 at the center point on C Light Source.

8. QUALITY ASSURANCE

No.	Test Items	Test Condition	Note
1	High Temperature Storage	70℃, 240hrs	Note 1, 2
2	Low Temperature Storage	-30℃, 240hrs	Note 1, 2
3	High Temperature Operation	70℃, 240hrs	Note 1, 2
4	Low Temperature Operation	-20℃, 240hrs	Note 1, 2
5	High Temperature and High Humidity Storage	60℃, 90%RH, 240hrs	Note 1, 2
6	Thermal Shock	-20℃/0.5h ~ +70℃/0.5h for a total 100 cycles	Note 1, 2
7	Electro Static Discharge	C=150pF,R=330Ω, 5point/panel Air:±4Kv, 5times	Note 2
8	Package Drop Test	Height:60cm,1 corner,3 edges,6 surfaces	Note 2

Note 1: The test samples have recovery time for 2 hours at room temperature before the function check. In the standard conditions, there is no display function NG issue occurred.

Note 2: After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

9. HANDING CAUTIONS

9.1 ESD (Electrical Static Discharge) strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommended ESD strategy

(1) In handling LCD panel, please wear gloves with non-charged material. Using the conduction ring connects wrist to the earth and the conducting shoes to the earth necessary is.

(2) The machine and working table for the panel should have ESD protection strategy.

(3) In handling the panel, ionized airflow decreases the charge in the environment is necessary.

(4) In the process of assemble module, shield case should connect to the ground.

9.2 Environment

(1) Working environment of the panel should be in the clean room.

(2) Because touch panel has protective film on the surface, please remove the protection film slowly with ionized air to prevent the electrostatic discharge.

9.3 Others

(1) Turn off the power supply before connecting and disconnecting signal input cable.

(2) Because the connection area of FPC and panel is not so strong, do not handle panel only by FPC or bend FPC.

(3) Water drop on the surface or condensation as panel power on will corrode panel electrode.

(4) As the packing bag open, watch out the environment of the panel storage. High temperature and high humidity environment is prohibited.

(5) In the case the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hands cleanly with water and soap as soon as possible.

(6) Unpacking (Hard Box) in order to prevent open cells broken:

[6.1] Moving hard boxes by one operator may cause hard boxes fell down and open cells broken by abnormal methods. Two operators carry one hard box with their two hands. Do handle hard boxes carefully, such as avoiding impact, putting down, and piling up gently.

[6.2] To prevent hard boxes sliding from carts and falling down, hard boxes should be placed on a surface with resistance.

[6.3] To prevent an open cell broken or a COF damaged in a hard box, please follow the instructions below:

[6.3.1] Do not peel a polarizer protection film of an open cell off in a hard box.

[6.3.2] Do not install FFC or LVDS cables of an open cell in a hard box.

[6.3.3] Do not press the surface of an open cell in a hard box.

[6.3.4] Do not pull X-board when an open cell placed in a hard box.

(7) Handling – In order to prevent open cells, COFs , and components damaged:

[7.1] The forced displacement between open cells and X-board may cause a COF damaged. Use a fixture tool for handling an open cell to avoid X-board vibrating and interfering with other components on a PCBA & a COF.

[7.2] To prevent open cells and COFs damaged by taking out from hard boxes, using vacuum jigs to take out open cells horizontally is recommended.

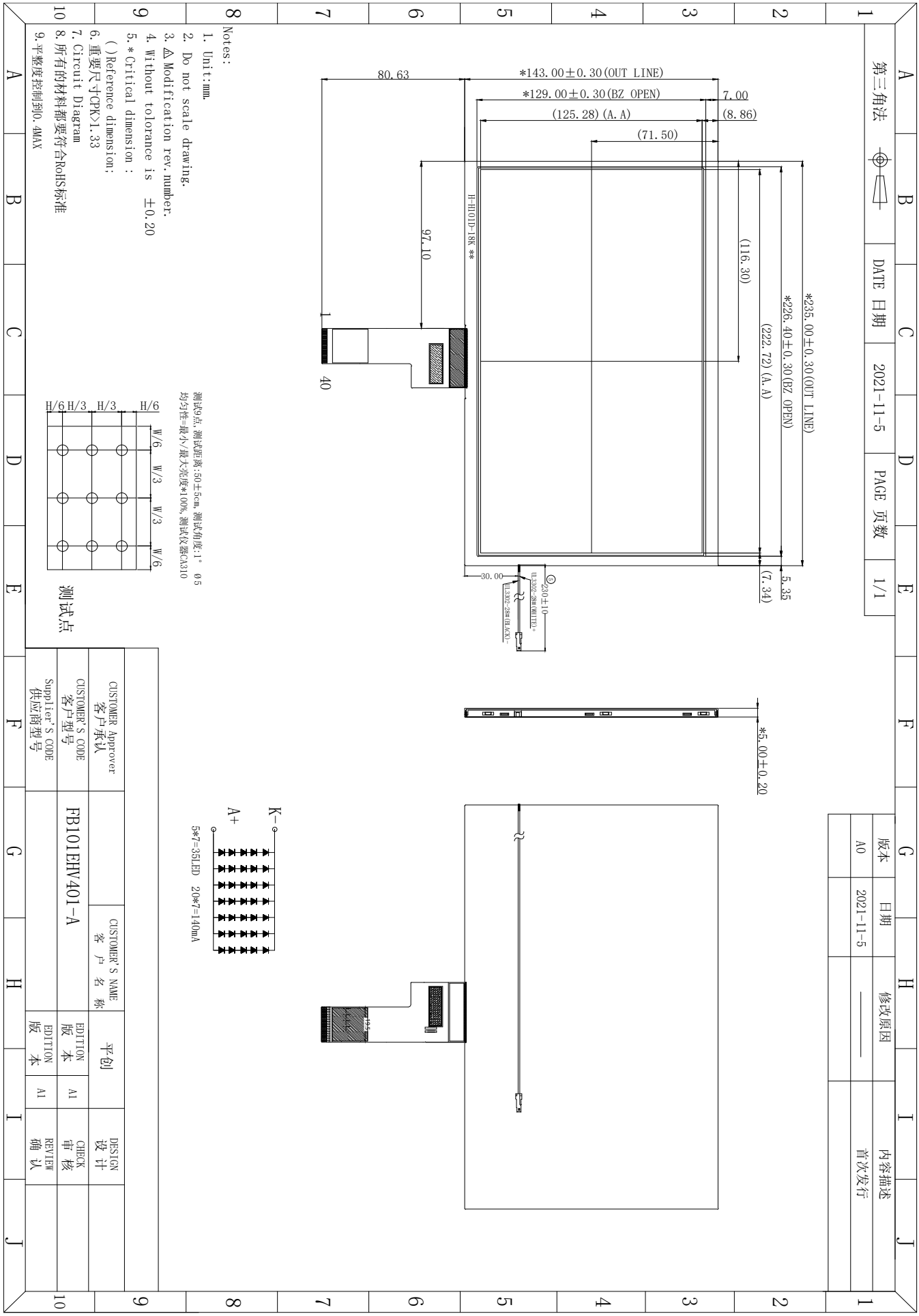
[7.3] Improper installation procedure may cause COFs of an open cell over bent which causes damages. As installing an open cell on a backlight or a test jig, place the bottom side of the open cell first on the backlight or the test jig and make sure no interference before fitting the open cell into the backlight/the test jig.

[7.4] Handle open cells one by one.

[7.5] In order to prevent driver IC from being injured by ESD, it is not recommended that the following positions be directly touched by hands.

(8) Avoid any metal or conductive material to contact PCB components, because it could cause electrical damage or defect.

10. MECHANICAL DRAWING



11. Packaging Drawing

11.1. Packaging Material Table

11.3. Packaging Drawing